IULIAN URSAC

Professional Experience

Product and component verification engineer – Infineon Technologies
Sep '14 until Present- Bucharest, Romania

Product Engineer
(Apr 2015 – May 2017)
Semiconductor product yield engineering and failure analysis for integrated circuits in the area of automotive applications with main focus on Motor drivers and System Basis Chips (SBC) with following responsibilities:

- Act as the interface between production, business division, engineering areas and quality management across different locations.
- Product field return failure analysis and production support in the case of issues
- Lot-on-hold analysis including risk assessment and lot disposition
- Support transfer and conversion projects (Data analysis of tested)
- Definition and execution of counter-measures in case of deviations
- Product monitoring during production lifetime (eg: Yield improvement based on cp/cpk analysis);
- Support "development to production" phase (eq. performing Qualification process)

Component Verification Engineer
(Sept 2014-May 2015 &June 2017 – present)

- IC Product validation and characterization in the area of automotive applications, System Basis Chips (SBC): Gate drivers, Motor Drivers, Low dropout voltage regulators, Current sense amplifier, Protections and Diagnostic.
- Define and execute electrical & functional test cases using automation (Matlab)

- *Key Technologies:*
  - Automotive, Data analysis, System Basis Chip, Gate drivers, Matlab scripting, Automate measurements

Mixed-Signal Design Engineer - Gryphon Development (EXAQTWORLD)
Apr '09 until Aug '14' - Bucharest, Romania

R&D centre of EXAQTWORLD French Company specialized on design anti-theft RFID solutions: UHF (840 – 960 MHz) RFID Smart Detacher & 8.2MHz anti-theft Mono-board
Responsibilities:

- Defining project requirements with System level concept development
- Create Schematic and Printed Circuit Board (PCB) layout
- Prototyping, Debug and validation
- Development of production test procedure

Project manager activities

- In parallel with the specific project tasks, also act as a Project Responsible being an interface between the Development team, business line and manufacturing (Suppliers, PCB factory, Assembly company)
- Identifying and solving project issues effectively
- Track progress and review project tasks
- Conduct regular status meetings
- Coordinate and facilitate delivery of project objectives

Key Technologies:

- RFID, Anti-Theft RF Electronic Article, OrCAD tool chain, Project management

Analogue and Mixed-Signal IC Design Engineer - AnSem International
Sep '08 until Dec '08 - Leuven, Belgium

AnSem International it is a Fabless semiconductor company specialized in offering IC design services

Responsibilities:

- Involved in library management, verification and simulation of complete design and RF sub-circuits
- Low power amplifier 0.18um for EKG sensor (<24uA)

Key technologies:

- Mixed Signal Design:
- 0.13 µm RF CMOS Integrated Circuit (SoC)

Radio Frequency Integrated Circuit Design Engineer - AsicAhead International
Aug '05 until Sep '08- Bucharest, Romania

AsicAhead International is an IC Design Company HQ in Belgium, with R&D site in Bucharest

Team leader Activities:

- Responsible for integration of fully reconfigurable IBM 0.13um CMOS, 0.13GHz - 6GHz WiMAX Transceiver(IEEE 802.16 SoC)
- TOP level Schematic Design (mixer, buffer, power amplifier chain)

Analogue Design Experience:

- 0.13GHz - 6GHz Frequency Synthesizer: Design, Simulation and Layout floor plan (Freq. synthesizer top level, VCO, phase frequency detector, charge pump)
- TX power amplifier Simulations and Layout
- Quadrature local oscillator design: Clock buffer tree ; layout and design
- 3.5GHz Up conversion Mixer: Design and Layout
- 2GHz up to 6GHz frequency multiplier

Laboratory Experience:

- 0.13 to 6 GHz Frequency Synthesizers characterisation
- 0.13GHz - 3.5GHz Transmitter EVM(Error Vector Magnitude) measurements

Key Technologies:

- IEEE802.16, WiMAX Software Defined Radio
- 0.13 µm RF CMOS Integrated Circuit (SoC)
- 6GHz Radio frequency (RF) synthesizer, Spectrum analyser
- Cadence tool chain

Analogue Design (working student) - AsicAhead International
Aug '04 until May '05 – Iasi, Romania

Responsibilities: "CMOS 0.13 um, 500 MHz LPF Cut-off frequency Gm-C Active Filter "(Cadence ICFB designer: Virtuoso schematic & Spectre simulations)

Education

Ph. D study 2017-2021

University "Politehnica"- Bucharest
Thesis subject:
802.11g standard Wireless Radio Communications Frequency Synthesizer

M.Sc. study - 2005 until Feb 2007

University "Politehnica"- Bucharest in Partnership with Infineon Technologies Romania&CO SCS (Lectors Georg Pelz and Heinz Zitta)
Faculty of "Electronics Telecommunications and Technology of Information"
Department of "Advanced Microelectronics"
Thesis subject: "Frequency Synthesizer using Digital Controlled Oscillator"

B.Sc. study - 2000 until 2005

Technical University "Gh. Asachi"- Iasi
Faculty of "Electronics and Telecommunications"
Department of "Microelectronics"
Thesis subject: "500MHz Active Low Pass Filter"

College - 1996 until 2000
Industrial College "Stefan Procopiu"- Vaslui,
Department of "Telecommunications"
Title: Manufacturer of electronic and telecommunications products

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Courses

Jan'07- June'07	**Project Management course:** MTZ865 (Bucharest) CODECS (Romania) with "Open University" (UK)
Sept'14- Nov'20	**Infineon internal trainings** (Bucharest) Management, Failure Analysis
Sept'08- Nov'08	**Ansem internal trainings** (Leuven – Belgium) Matlab, IC digital design, IC analogue design, IC layout, VHDL-AMS, ISO9001
June'07	**Cadence Virtuoso Layout** (Paris, France)
'00 – '04	**Teaching Courses (**Technical University "Gh. Asachi"- Iasi, Romania)

Hardware relevant skills (relevant tools used as engineer)

Cadence Tools:
- ICFB designer:
  - Schematic Editor & Virtuoso Layout
  - SpectreRF, SpectreSverilog, UltraSim
  - Diva/Assura (DRC, LVS, Parasitic Extract, Floating Metals, Global Density)
- OrCAD: Capture CIS, PSpice AD, Layout Plus.

Mentor Graphics Tools:
- Eldo and Eldo RF simulators;
- Modelsim:VHDL, Verilog, Veriloga.

Agilent Technologies: Advanced Design System
Tanner Tools: L-Edit, S-Edit.

Software relevant skills

- Mathworks: Matlab scripting and Simulink
- VHDL, Verilog
- Boarland C
- Assembler (beginer)

Research/Projects

0.18um TSMC DAC Compensation technique. Production prototype (2014)

Research Grant ('09 – '11)
SELECTING OPTIMUM TEST FREQUENCY IN DICTIONARY OF FAULT TECHNIQUES
The paper deals with diagnosis of soft faults for analogue circuits in simulation after test approach. The values of the parameters for linear circuits are identified employing approximate symbolic pole/zero and gain vs. frequency characteristics.

Publications

[1] Iulian Ursac, Florin Constantinescu "*A New Dual Loop Frequency Synthesizer for the Wireless Standard 802.11g*", International Symposium on Fundamentals of Electrical Engineering, November 5-7 2020, University Politehnica of Bucharest, Romania.

[2] Iulian Ursac, Florin Constantinescu "*Calibration of the Frequency Reference for the Communications Standard 802.11g*", International Symposium on Fundamentals of Electrical Engineering, November 5-7 2020, University Politehnica of Bucharest, Romania.

[3] Iulian Ursac, Florin Constantinescu, Mihai Marin, "*A frequency reference for carrier synthesis in wireless standard 802.11g"*, Scientific Bulletin of the Electrical Engineering Faculty – Year 20 No.1 (42) ISSN 2286-2455, September 2020 **DOI: 10.2478/SBEEF-2020-0112**

[4] Mihai-Eugen Marin , Catalin Brinzei, Florin Constantinescu,Alexandru Gheorghe,Iulian Ursac, "*Design of a 8 bit current steering DAC for a GSM transmitter"*, International Symposium on Fundamentals of Electrical Engineering, November 28-29 2014, University Politehnica of Bucharest, Romania. **INSPEC: 14949280**
https://ieeexplore.ieee.org/abstract/document/7050565?section=abstract

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